Design of a CMOS High Dynamic Range Automatic Gain Control System for Telecommand Applications

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Abstract

Automatic Gain Control circuits are closed loop control systems that are widely used in telecommand applications for avionic systems and other receivers to maintain a constant output signal level despite variation of signal amplitude at its input. This paper presents the design of an analog Automatic Gain Control System using AMS-0.35µm CMOS technology at 3.3V supply voltage for a frequency of 10.7 MHz with a desired output level at -10dBm for an input dynamic range of -85dBm to +3dBm. The system consists of 50Ω matched single-ended input and output variable gain amplifier whose gain is automatically adjusted with the control voltage generated in the feedback loop. The feedback loop consists of a low power CMOS RF power detector and a control voltage generator. The RF Power detector consists of an RMS power detector and a sequence of limiting amplifiers operating as a logarithmic detector. The RF power detector has a dynamic range of -60dBm ~ -10dBm. The control voltage generator used in this system is a square-law based consisting of a single transistor, thereby saving the chip space to a great extent. The AGC gain ranges from 71.4dB ~ -9.43dB with an output level accuracy of ± 3.5dB. The proposed AGC system has a very high input dynamic range.

Introduction

Many industries use RF communication including television broadcasting, radar systems, remote control, remote metering/monitoring and so on. Due to atmospheric attenuations (such as scattering and absorption in the ionosphere, phase fluctuations, field strength variations with distance and height, effect of earth's curvature, received signal fading conditions), the receiving antenna's input will fluctuate along a wide range of values that will cause the output signal to undergo great changes. In RF communication, variations in the signal amplitude at the receiver's input (termed as fading), requires continuous alteration in the gain of the receiver so as to maintain a relatively constant output signal. In order to get the best possible SNR at the receiver output, the signal intensity must be kept within an acceptable range. This led to the design of circuits, which are capable of maintaining a relatively constant output signal despite variations at the input of the system. Those circuits were described as Automatic Volume Control (AVC) circuits, which after a few years were generalized under the name of Automatic Gain Control (AGC) circuits.

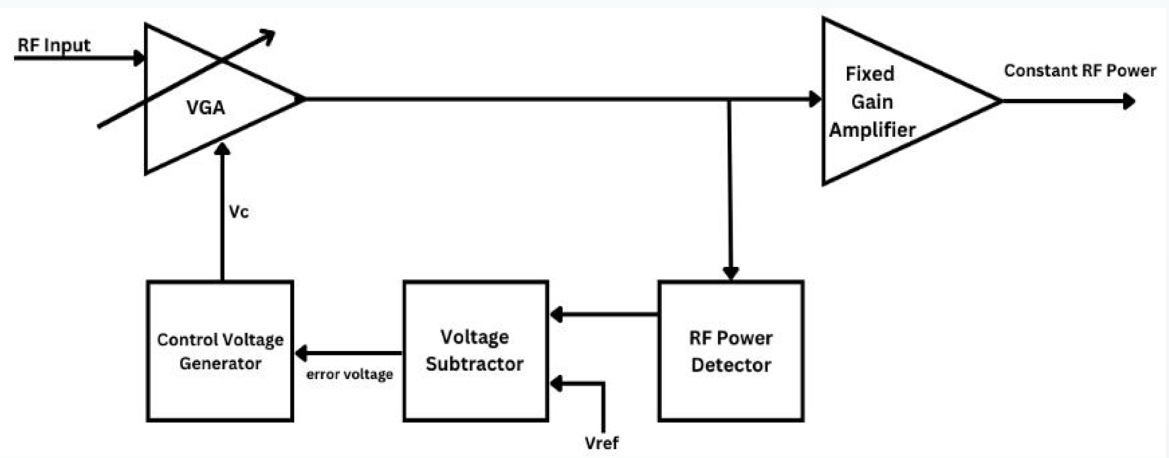
The command sent to control a system from a remote location is called a telecommand. In avionic systems, telecommand is used to destruct the launch vehicle in case of large deviation from the expected trajectory. Telecommand frequency is downconverted to an IF of 10.7MHz using a super heterodyne architecture.

For any communication system, good control and selectivity of the output signal level is essential. But practically, this is a fundamental issue that is being faced in the design of any communication system. To tackle this, nowadays, AGC circuits can be found in every communication system where large fluctuations in the output signal leads to loss of information or to an undesirable performance of the system

AGC Design Specifications

CMOS Technology - 0.35um C35B4M3
Foundry - AMS
IF - 10.7 MHz
50 Ohm single-ended input-output
Input Power range - -85dBm ~ +3dBm
Output power - -10dBm.

Proposed System - Block Diagram



Design Methodology

1. The proposed AGC system is designed in Cadence Design Environment using 0.35µm CMOS technology from AMS Foundry.
2. A 50 Ohm matched single-ended input-output Variable Gain Amplifier that consists of a differential cascode structure with constant tail current source and active inductive load is designed as shown in Fig.1.
3. Low pass composite microwave filter was designed as shown in Fig.2 to attenuate the unwanted harmonics at the VGA output
4. A RF power detector consisting of a RMS Power detector and Logarithmic limiting amplifier stages is designed as shown in Fig.3 and Fig.4 respectively.
5. The detected power is compared with a reference voltage using a voltage subtractor and an error voltage is generated.
6. The output of the difference amplifier is the error voltage value which has to be mapped to the required control voltage.
7. A VVC (Voltage to Voltage Converter) which works as a square law based control voltage generator (Fig.5) is used to map these values.
8. Fixed Gain Amplifier stages (same architecture as VGA) are used after VGA output to get the desired RF output power at -10dBm.

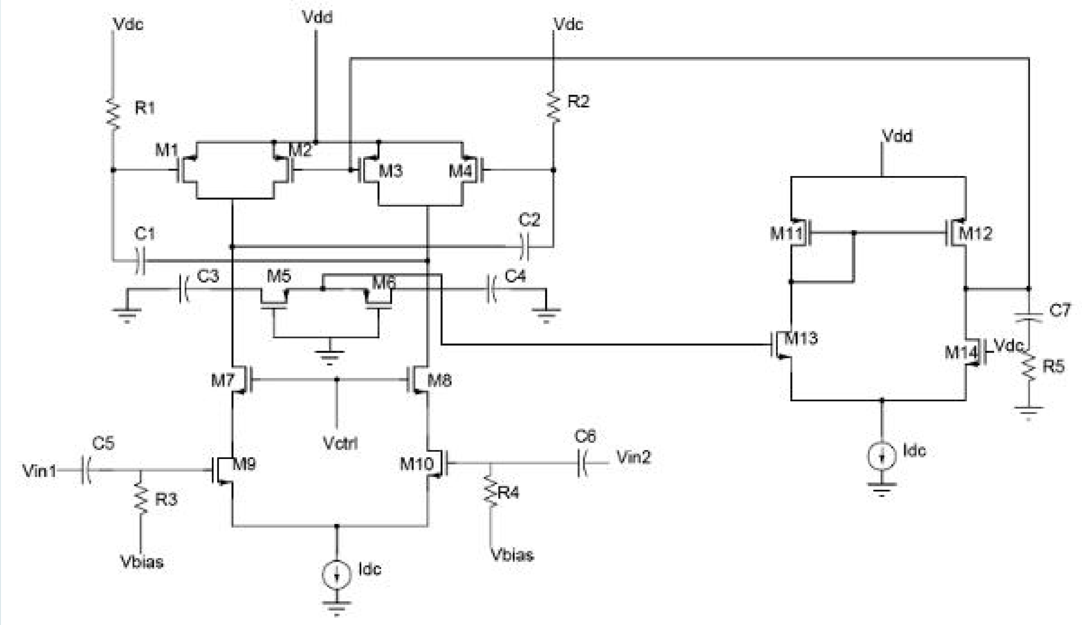


Fig.1. VGA with CMFB

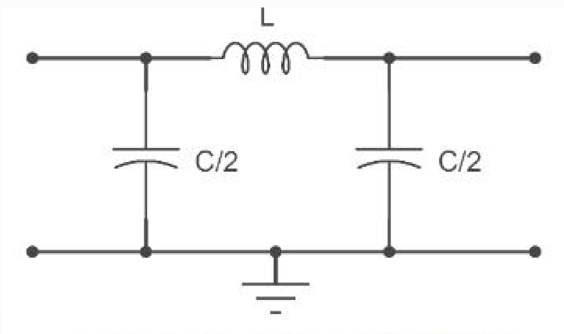


Fig.2. Low pass composite microwave filter

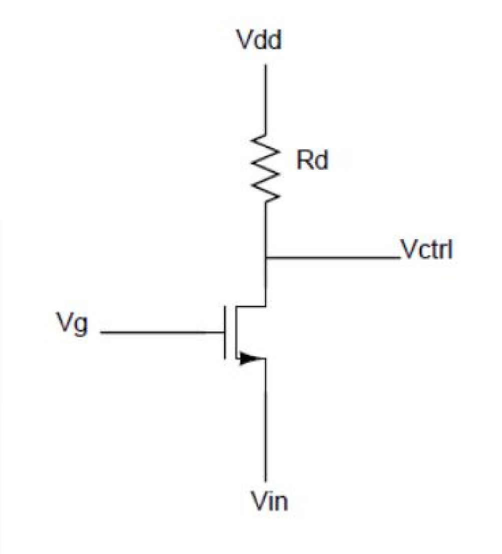


Fig.5. VVC (Control Voltage Generator)

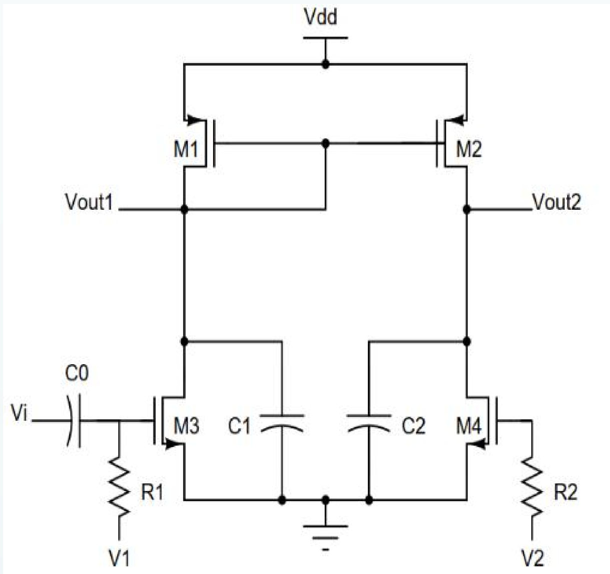


Fig. 3. RMS power detector

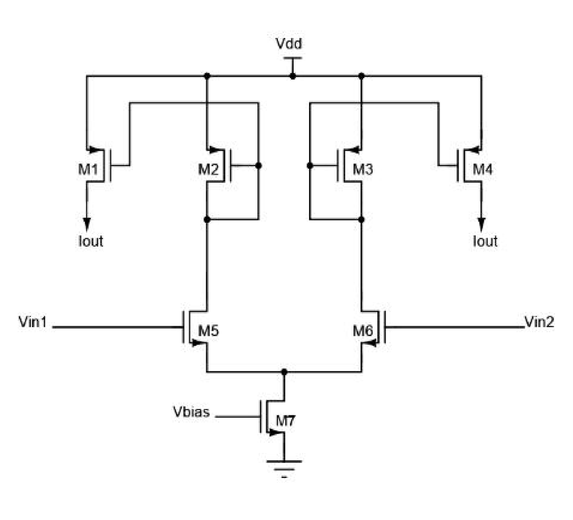
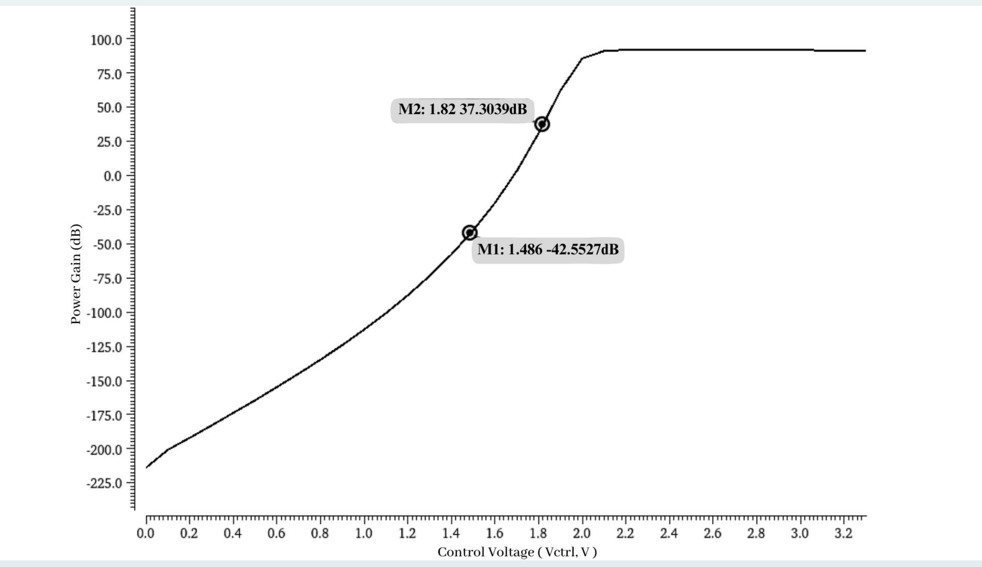


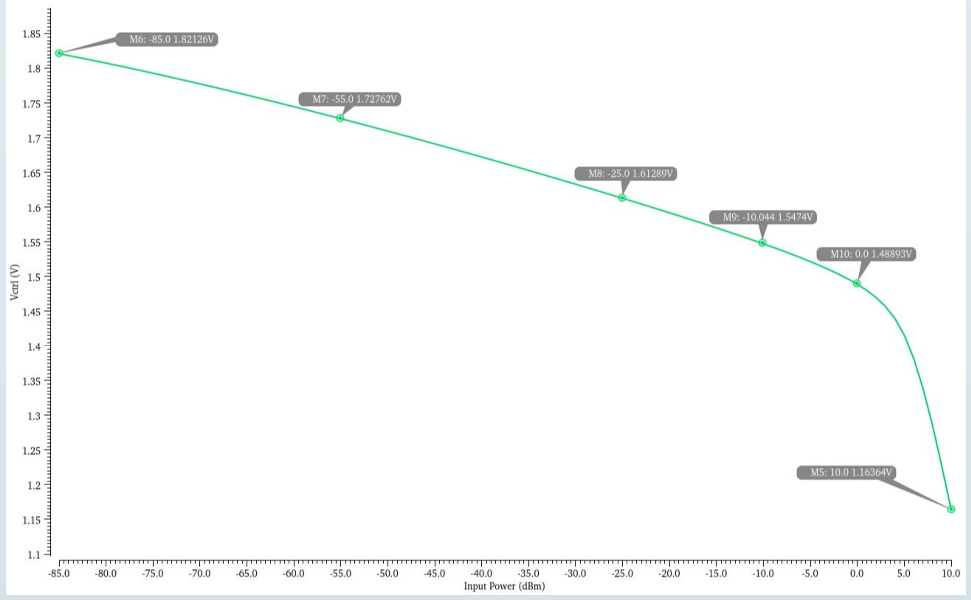
Fig.4. Logarithmic amplifier

Results

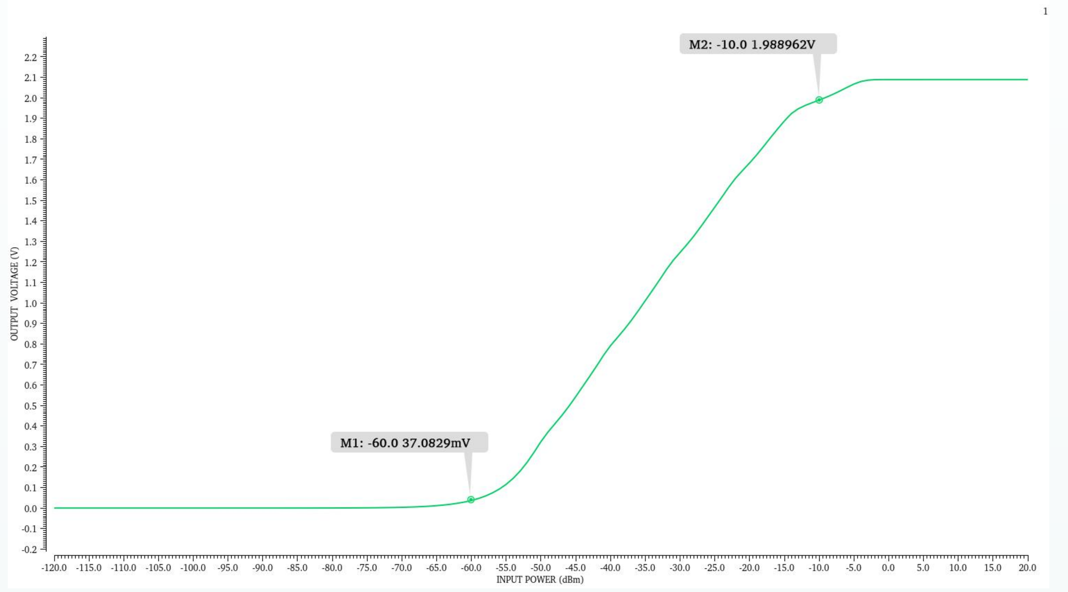
- VGA Gain range for -60dBm input power



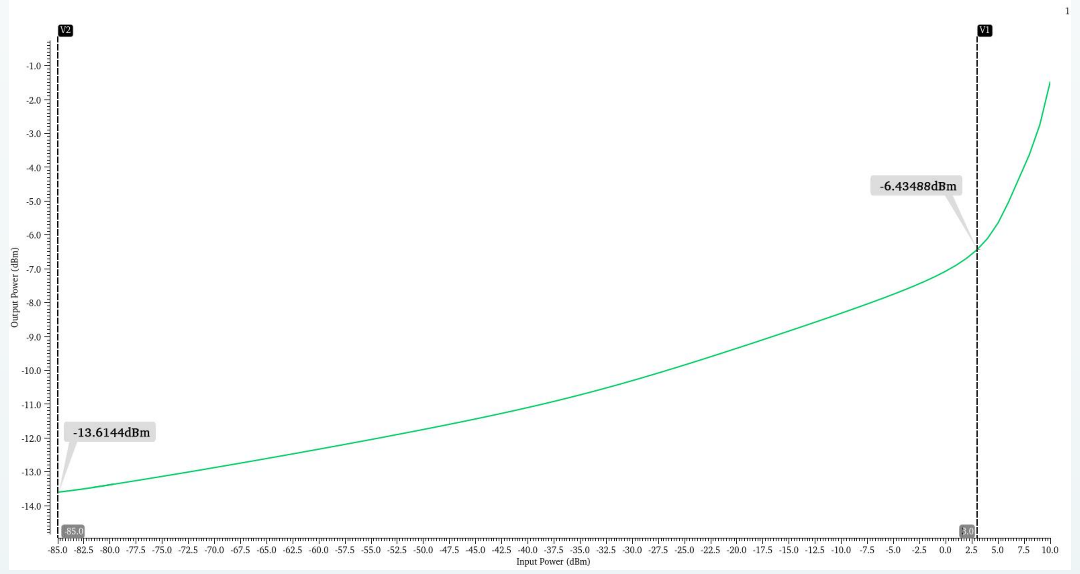
- Input Power vs Control Voltage (AGC)



- Differential output voltage vs Input power (RF power detector)



- AGC Final RF Power at -10dBm (Accuracy ±3.5 dB)



Performance Summary

Parameters	Simulation Results
CMOS Process	0.35µm
Supply Voltage(V)	3.3
Operating Frequency(Hz)	10.7M
Dynamic range(dBm)	-85 ~ +3
AGC Gain(dB)	71.4 ~ -9.43
Output Level(dBm)	-10
Output Level Accuracy(dB)	±3.5
VGA	
VGA Gain(dB)	-42.56 ~ 37.3
Power consumption(mW)	911.856
RF Power Detector	
Input detectable range(dBm)	-60 ~ -10
Output voltage range(V)	37.082m ~ 1.9889
Power consumption(mW)	66.18

Conclusion

This study is devoted to outlining the design of an analog Automatic Gain Control System using AMS-0.35µm CMOS technology at 3.3V supply voltage at a frequency of 10.7MHz with a desired output level of -10dBm for an input dynamic range of -85dBm to +3dBm. The gain of VGA is automatically adjusted using the control voltage generated in the feedback loop. A control voltage generator and a low power CMOS RF power detector make up the feedback loop). Here, a square-law generator with only one transistor is the circuit in operation, which substantially minimizes the amount of chip area required. All of the algorithms mentioned above have been put into practise and successfully tested, and the results produced by these methods have satisfied all the required specifications .